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Applicant	:	Andrew W. Martwick	
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Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant submits, the following Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith our check number 0192 in the amount of $500 to cover the cost of filing the opening brief as required by 37 C.F.R. § 41.20(1)(b). Please charge any additional fees or credit any overpayment to our deposit Account No.02-2666. A duplicate copy of the Fee Transmittal is enclosed for this purpose.

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-30 of the present application are pending and remain rejected. The Applicants hereby appeals the rejection of claims 1-30.

IV. STATUS OF AMENDMENTS

The Applicant filed an amendment on January 27, 2005, in response to an Office Action issued by the Examiner on November 30, 2004. In response to the January 27, 2005 amendment, the Examiner issued Final Office Action on June 13, 2005. The Applicant filed a Notice of Appeal on September 13, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Independent Claims 1, 11, and 21:

The present invention is a method and apparatus for self-updating a firmware device. A computer system 100 includes, among other things, a processor 105, a host bus 110, and a host bridge chipset 120[1]. The host bridge chipset 120 includes a memory controller 122, a self-update controller 124, a firmware device 126, and an I/O controller 128[2]. A self-update controller 124 includes a communication interface 210, a source selector 220, a parser 230, a control logic circuit 240, and a read buffer 250[3].

The communication interface 210 provides an interface to a serial data stream. The serial data may come from a remote device via a modem, or from a test or programming

[1] See Specification, page 5, lines 21-24; Figure 1 (element 120).
[2] See Specification, page 6, lines 10-11; Figure 1 (element 124 and 126).
[3] See Specification, page 8, lines 8-11; Figure 2 (elements 210 and 230).

equipment. The serial data contains the programming information to update the firmware device[4]. The update data may include the boot code in a Basic Input/Output System (BIOS)[5].

The parser 230 decodes the data provided by a multiplexer 224[6] in the source selector 220. The parser 230 reads the program information and extracts the program parameters based on a known protocol and/or format[7].

2. Dependent Claims 2-9, 12-19, and 22-29:

The control logic circuit 240 includes an erase control circuit 242 and a write control circuit 244. The erase control circuit 242 generates signals to erase the firmware device. The write control circuit 244 generates signals to program or write the firmware device[8]. The read buffer 250 stores the program data received from the communication interface 210 and forwarded by the parser 230[9].

The source selector 220 selects the source for the input to the parser 230. There are essentially two sources: the parallel data from the communication interface 210 and the I/O interface data from the LPC bus. The source selector 220 includes a multiplexer controller 222 and a multiplexer 224. The multiplexer 224 is a two-to-one data selector to select one of the LPC interface data and the parallel data. The LPC interface data contains information for a normal operation. The parallel data contains the program information that is used to update the firmware device[10].

The programming information includes the self-update identifier, program parameters, and program data[11].

The parser is implemented by a state machine having an identification state 310, a program parameters read state 320, a program data buffer state 330, a block erasure state 340, a block write state 350, a status update state 360, and a normal operation state 370[12]. In the block erasure state 340, the state machine 300 performs the block erasure operation. The state machine 300 generates control signals to the erase control circuit 242 to erase the

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[4] See Specification, page 8, lines 12-15.
[5] See Specification, page 8, lines 22-23.
[6] See Specification, page 10, line 3.
[7] See Specification, page 11, lines 4-6; Figure 3 (element 320).
[8] See Specification, page 10, lines 7-10; Figure 2 (element 240).
[9] See Specification, page 10, lines 11-17; Figure 2 (element 250).
[10] See Specification, page 9, lines 11-18.
[11] See Specification, page 8, lines 15-16.
[12] See Specification, page 10, lines 18-22; Figure 3.

firmware device at the specified erase block address[13]. After the erasure is completed, the state machine 300 transitions to the block write state 350. In the block write state 350, the state machines 300 generates control signals to the write control circuit 244 to write the data in the read buffer 250 to the firmware device at the specified write block address[14].

The communication interface 210 includes a receiver interface 212 and a serial-to-parallel converter 214. The serial-to-parallel converter 214 converts the serial data stream into parallel data. The parallel data may be of any size comparable with the parser[15].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1, 11, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cooper in view of Estakhri.

(2) Claims 2-9, 12-29, and 22-29 rejected under 35 U.S.C. § 103(a) as being unpatentable over Cooper and Estakhri and further in view of Tanaka.

VII. ARGUMENTS

A. Claims 1, 11, and 21 Are Not Obvious under 35 U.S.C. § 103(a) as being unpatentable over Cooper in view of Estakhri

In the Final Office Action, the Examiner rejected claims 1, 11, and 21 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,805,882 issued to Cooper et al. ("Cooper") in view of U.S. Patent No. 5,606,660 issued to Estakhri et al. ("Estakhri"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend

[13] See Specification, page 11, lines 20-23.
[14] See Specification, page 11, lines 24-25; page 12, lines 1-3.
[15] See Specification, page 9, lines 1-10.

that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Cooper discloses a computer system and method for replacing obsolete or corrupt boot code contained within a flash ROM. The flash ROM is connected to a mobile super I/O (MSIO) chip and the MSIO is connected to a system controller (Cooper, col. 5, lines 29-31).

Estakhri discloses a method and apparatus for combining controller firmware storage and controller logic in a mass storage system. A controller 300 includes a buffer 310 through which data or firmware code is transferred bi-directionally between flash memory 200 and host system 400 through a PCMIA interface (Estakhri, col. 3, lines 17-21). A ROM 330 contains primitive microprocessor code for downloading firmware from flash sectors 200 to RAM 320 in addition to code for checking the integrity of the downloaded code (Estakhri, col. 3, lines 28-32).

Cooper and Estakhri, taken alone or in any combination, do not disclose, suggest, or render obvious (1) receiving programming information to update a firmware device containing a boot code for a processor in a chipset separated from the processor from a communication interface, and (2) parsing the programming information into control commands and program data by a parser. There is no motivation to combine Cooper and Estakhri because neither of them addresses the problem of updating a firmware device in a chipset separated from the processor. There is no teaching or suggestion that a chipset separated from the processor is present. Cooper merely discloses replacing obsolete boot code. Cooper does not disclose a chipset. Estakhri merely discloses a ROM containing a microprocessor code. A ROM is not capable of being updated. Furthermore, Estakhri does not disclose or suggest that the ROM or the flash sectors 200 contains a boot code. Cooper, read as a whole, does not suggest the desirability of updating a boot code in a chipset.

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452,

1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Furthermore, although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills 916 F.2d at 682, 16 USPQ2d at 1432; In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992). When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Col, Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

In the present invention, the cited references do not expressly or implicitly suggest updating a boot code in a chipset. In addition, the Examiner failed to present a convincing

line of reasoning as to why a combination of Cooper and Estakhri is an obvious application of self-updating a firmware device in a chipset separated from the processor.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references.

B. Claims 2-9, 12-29, and 22-29 Are Not Obvious under 35 U.S.C. § 103(a) as being unpatentable over Cooper and Estakhri and further in view of Tanaka

In the Final Office Action, the Examiner rejected claims 2-9, 12-29, and 22-29 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,805,882 issued to Cooper et al. ("Cooper") in view of U.S. Patent No. 5,606,660 issued to Estakhri et al. ("Estakhri") and further in view of U.S. Patent No. 6,266,810 issued to Tanaka et al. ("Tanaka"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Cooper and Estakhri are discussed above regarding claims 1, 11, and 21.

Tanaka discloses a remote program downloading system and apparatus. A program acquiring means reads a packet into a buffer memory (Tanaka, col. 6, lines 14-19). A program storing means stores only the program main body into a flash ROM on the basis of the information in the buffer (Tanaka, col. 6, lines 20-24).

Cooper, Estakhri and Tanaka, taken alone or in any combination, do not disclose, suggest, or render obvious, at least, (1) receiving programming information to update a firmware device containing a boot code for a processor in a chipset separated from the processor from a communication interface, (2) parsing the programming information into control commands and program data by a parser, (3) programming the firmware device

based on control commands by control logic circuit, (4) storing the program data in a buffer, (5) selecting one of the programming information and an I/O channel data by a multiplexer, (6) recognizing self-update identifier, (7) reading program parameters, etc., and (8) converting serial data into the programming information by a serial to parallel converter. There is no motivation to combine Cooper, Estakhri and Tanaka because none of them addresses the problem of updating a firmware device in a chipset separated from the processor. There is no teaching or suggestion that a chipset separated from the processor is present. Cooper merely discloses replacing obsolete boot code. Cooper does not disclose a chipset. Estakhri merely discloses a ROM containing a microprocessor code. A ROM is not capable of being updated. Furthermore, Estakhri does not disclose or suggest that the ROM or the flash sectors 200 contains a boot code. Tanaka merely disclosed a buffer memory storing address and size information, not actual program data. Tanaka merely discloses reading the program control information into its own buffer memory (Tanaka, col. 4, lines 41-45). This is not the same as storing the program data in a buffer. Cooper, read as a whole, does not suggest the desirability of updating a boot code in a chipset.

Regarding claims 9, 19, and 29, the Examiner states that Cooper and Estakhri do not disclose converting serial data in to the programming information by a serial to parallel converter. The Examiner then contends that Tanaka implicitly teaches converting serial data by a serial to parallel converter (Final Office Action, page 7, paragraph number 14). Applicant respectfully disagrees. First, as the Examiner pointed out, both Cooper and Estakhri disclose receiving the programming information in parallel form. Therefore, Cooper and Estakhri both teach away from using serial data. It is improper to combine references where the references teach away from their combination. In re Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). Second, Tanaka does not disclose converting serial data. Tanaka merely discloses a packet stream. A packet stream merely a stream of packets and has nothing to do with converting serial data. Apparently, the Examiner reaches that conclusion based on the theory of inherency. However, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 193). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing

described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). Here, Tanaka does not disclose converting serial data using a serial-to-parallel converter. The fact that a serial-to-parallel converter may be used is not sufficient to establish the inherency of that feature.

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Furthermore, although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills 916 F.2d at 682, 16 USPQ2d at 1432; In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992). When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Col, Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986)..

In the present invention, the cited references do not expressly or implicitly suggest at least any one of the above elements. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Cooper, Estakhri and Tanaka is an obvious application of self-updating a firmware device in a chipset separated from the processor.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references.

VIII. CONCLUSION

Applicant respectfully requests that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are not obvious over the cited prior art references.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: December 8, 2005

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IX. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (previously presented) A method comprising:

receiving programming information to update a firmware device containing a boot code for a processor in a chipset separated from the processor from a communication interface; and

parsing the programming information into control commands and program data by a parser.

2. (original) The method of claim 1 further comprising:

programming the firmware device based on the control commands by a control logic circuit; and

storing the program data to be written into the firmware device in a buffer.

3. (original) The method of claim 2 further comprising:

providing the programming information to the parser by a source selector.

4. (original) The method of claim 3 wherein providing the programming information comprises:

selecting one of the programming information from the communication interface and an input and output (I/O) channel data by a multiplexer; and

controlling a selection of the multiplexer by a multiplexer controller.

5. (original) The method of claim 2 wherein programming the firmware device comprises:

erasing the firmware device by an erase control circuit; and

writing to the firmware device using the program data in the buffer by a write control circuit.

6. (original) The method of claim 2 wherein the parsing comprises:

generating the control commands based on the parsed programming information by a state machine, the control commands including at least an erase command and a write command.

7. (original) The method of claim 6 wherein the programming information includes at least a self-update identifier, program parameters, and the program data.

8. (original) The method of claim 7 wherein generating the control commands comprises:

recognizing the self-update identifier;

reading the program parameters including at least erase and write addresses;

generating a buffer write command to write the program data into the buffer;

generating an erase command to the erase control circuit to a block in the firmware device at the erase address; and

generating a write command to the write control circuit to the program data in the buffer to the firmware device at the write address.

9. (original) The method of claim 1 wherein receiving comprises:

converting serial data into the programming information by a serial to parallel converter.

10. (previously presented) The method of claim 4 wherein the I/O data channel is the low pin count (LPC) interface.

11. (previously presented) An apparatus comprising:

a communication interface to receive programming information to update a firmware device containing a boot code for a processor in a chipset separated from the processor; and

a parser coupled to the communication interface to parse the programming information into control commands and program data.

12. (original) The apparatus of claim 11 further comprising:

a control logic circuit coupled to the parser to program the firmware device based on the control commands; and

a buffer coupled to the parser to store the program data to be written into the firmware device.

13. (original) The apparatus of claim 12 further comprising:

a source selector coupled to the communication interface and the parser to provide the programming information to the parser.

14. (original) The apparatus of claim 13 wherein the source selector comprises:

a multiplexer to select one of the programming information from the communication interface and an input and output (I/O) channel data; and

a multiplexer controller coupled to the multiplexer to control a selection of the multiplexer.

15. (original) The apparatus of claim 12 wherein the control logic circuit comprises:

an erase control circuit to erase the firmware device; and

a write control circuit to write the firmware device using the program data in the buffer.

16. (original) The apparatus of claim 12 wherein the parser comprises:

a state machine to generate the control commands based on the parsed programming information, the control commands including at least an erase command and a write command.

17 (original) The apparatus of claim 16 wherein the programming information includes at least a self-update identifier, program parameters, and program data.

18. (original) The apparatus of claim 17 wherein the state machine comprises:

a self-update identification state to recognize the self-update identifier;

a program parameters read state coupled to the self-update identification state to read the program parameters including at least erase and write addresses;

a program data buffer state to generate a buffer write command to write the program data into the buffer;

a block erasure state to generate the erase command, the erase command causing the erase control circuit to erase a block in the firmware device at the erase address; and

a block write state to generate the write command, the write command causing the write control circuit to write the program data in the buffer to the firmware device at the write address.

19. (original) The apparatus of claim 15 wherein the communication interface includes a serial to parallel converter to convert serial data into the programming information.

20. (previously presented) The apparatus of claim 14 wherein the I/O data channel is the low pin count (LPC) interface.

21. (previously presented) A system comprising:

a processor;

a firmware device; and

a self-update firmware controller coupled to the firmware device to self update the firmware device, the controller comprising:

a communication interface to receive programming information to update a firmware device containing a boot code for the processor in a chipset separated from the processor, and

a parser coupled to the communication interface to parse the programming information into control commands and program data.

22. (original) The system of claim 21 wherein the controller further comprising:

a control logic circuit coupled to the parser to program the firmware device based on the control commands; and

a buffer coupled to the parser to store the program data to be written into the firmware device.

23. (original) The system of claim 22 wherein the controller further comprising:

a source selector coupled to the communication interface and the parser to provide the programming information to the parser.

24. (original) The system of claim 23 wherein the source selector comprises:

a multiplexer to select one of the programming information from the communication interface and an input and output (I/O) channel data; and

a multiplexer controller coupled to the multiplexer to control a selection of the multiplexer.

25. (original) The system of claim 22 wherein the control logic circuit comprises:

an erase control circuit to erase the firmware device; and

a write control circuit to write the firmware device using the program data in the buffer.

26. (original) The system of claim 22 wherein the parser comprises:

a state machine to generate the control commands based on the parsed programming information, the control commands including at least an erase command and a write command.

27. (original) The system of claim 26 wherein the programming information includes at least a self-update identifier, program parameters, and program data.

28. (original) The system of claim 27 wherein the state machine comprises:

a self-update identification state to recognize the self-update identifier;

a program parameters read state coupled to the self-update identification state to read the program parameters including at least erase and write addresses;

a program data buffer state to generate a buffer write command to write the program data into the buffer;

a block erasure state to generate the erase command, the erase command causing the erase control circuit to erase a block in the firmware device at the erase address; and

a block write state to generate the write command, the write command causing the write control circuit to write the program data in the buffer to the firmware device at the write address.

29. (original) The system of claim 25 wherein the communication interface includes a serial to parallel converter to convert serial data into the programming information.

30. (previously presented) The system of claim 24 wherein the I/O data channel is the low pin count (LPC) interface.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.